Performance Investigation of Self-Lift and Re-Lift Luo Converter Topologies.

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ABSTRACT

This paper presents the Luo Converter topologies operating with simplified control loop algorithm for high voltage applications. Traditional DC-DC Boost Converters are used in high voltage applications, but they are not economical due to the limited output voltage, efficiency and require two sensors with complex control algorithm. Moreover due to the effect of parasitic elements, the output voltage and power transfer efficiency of DC-DC converters are limited. The voltage lift technique opens a good way to improve the performance characteristics of DC-DC converter.

The voltage lift technique for DC-DC converter is analyzed with simplified closed loop algorithm. The converter is operated in both line and load disturbance to analyze its feasibility of operation to maintain fixed output voltage. These converters perform positive DC-DC voltage increasing conversion with high power density, high efficiency, low cost in simple structure. They are different from other existing DC-DC step-up converters and possess many advantages including higher output voltage with small ripples and wide range of control. Theoretical analysis and simulation results are provided to verify its performance.

(Keywords: Luo converter, PI controller, Zigler Nicholas technique, boost converter, voltage lift technique)

INTRODUCTION

Traditional DC-DC Boost Converters are used in high voltage applications but they are not economical due to the limited output voltage, efficiency and require two sensors with complex control algorithm. Because of the effect of parasitic elements, the output voltage and transfer efficiency of DC-DC converters are limited. Luo-converters were used for the first time when Fang Lin Luo successfully applied the voltage lift technique for DC-DC converter to operate as boost mode [1]. The voltage lift technique is a technique applied in lifting the output voltage without using any external circuit, just by using the passive components [2]. It is a popular method widely applied in electronic circuit design. It has been successfully employed in DC-DC converter applications in recent years, and opened a good way to design high voltage gain converters. The output voltage increases stage-by-stage along the geometric progression. So to overcome the limitations of normal DC-DC converter and to make it with a simple control loop, a new technique called voltage lift technique is used [3].

A new series of DC-DC converter topology is analyzed which is different from conventional boost converter and they are:

1. Self-lift topology
2. Re-lift topology

For the analysis purpose the above topologies are to be simulated in MATLAB®/Simulation Software to verify its performance with line and load disturbances. A PWM algorithm is developed for the N-channel MOSFET switch is illustrated for the boost operation.

Self-Lift Circuit

Self-lift circuit [4] is derived from the normal buck converter circuit and it is shown in Figure 1. Self-Lift circuit is a boost converter circuit with the voltage lift components (i.e., an additional inductor and capacitor along with the basic circuit).

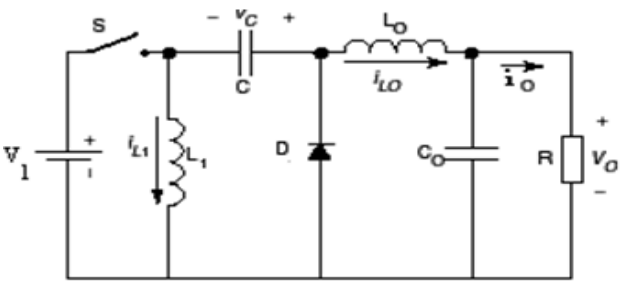

Figure 1: Self-Lift Topology.

It consists of passive components such as one static switch S, Diode D, two inductors L_1, L_2 and capacitors C_1, and C_2. Comparing with normal boost converter, it can be seen that there are only one more capacitor C_1, inductor L_1 and diode D_1 added into the self-lift circuit. Capacitor C_1 performs the characteristics to lift the capacitor voltage V_{C1} by a source voltage V_S.

In self-lift the switch S is N-channel power MOSFET device. It is driven by a pulse-width-modulated (PWM) switching signal with variable frequency f and conduction duty k. For this circuit, the load is usually resistive, R = Vo/Io.

The basic principle of self-lift circuit in boosting up the output voltage is, charging and discharging reactive elements into a load, controlling the levels of charge and consequently the output voltage by switching the DC supply in and out of the circuit at high frequencies. They include a freewheeling diode to protect the switch from the inductors high reverse currents, and this also ensures that the generated inductor energy is applied to the load. Capacitors are connected in parallel with the load to filter output ripple and maintain a constant output voltage.

Circuit Operation

When switch S is ON, its equivalent circuit is shown in fig.2.3. The source instantaneous current i_s is equal to $i_{L1} + i_{L2}$. Inductor L_1 absorbs energy from the source. Simultaneously inductor L_2 absorbs energy from the source and capacitor C. Both currents i_{L1} and i_{L2} increase during switch-ON period. The addition of input voltage and the capacitor voltage Vc1 that is stored in it during switch-OFF period supply load current.

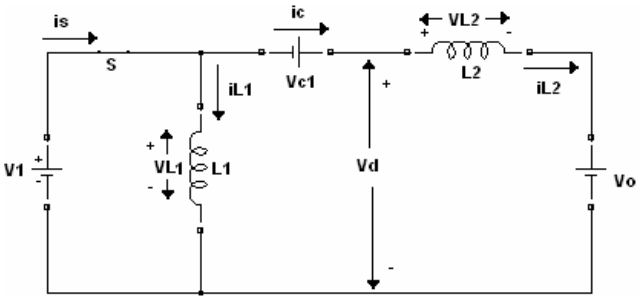

Figure 2: Switch-ON Equivalent Circuit.

When switch S is off, the source instantaneous current i_S=0. Current i_{L1} flows through diode D and charge capacitor C_1. Inductor L_1 transfers its stored energy to capacitor C_1 is shown in Figure-2.4. Simultaneously current i_{L2} flows through the load, which is sustained by the inductor L_2. Both currents i_{L1} and i_{L2} decrease during switch-OFF period.

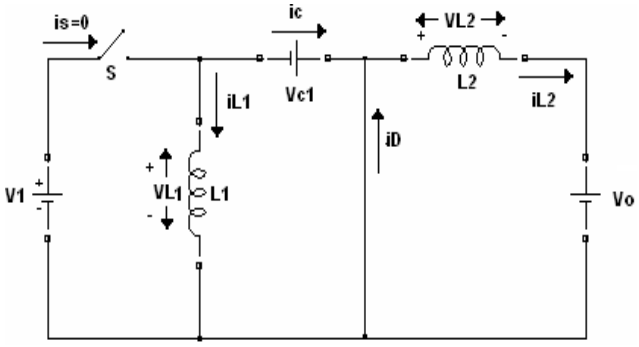

Figure 3: Switch-OFF Equivalent circuit

Analysis of Proposed Converter Self-Lift

In steady state, Self-lift circuit is shown in Figure-2.1 the average inductor voltages over a period are zero. Thus,

$$Vc_0=V_0 \qquad \textbf{(1)}$$

The inductor current I_L, increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_1 and V_{c1}. Therefore,

$$kTV_I = (1- k)\, TVc_1 \qquad \textbf{(2)}$$

Hence, during switch-on period, the voltage across capacitor C1 are equal to the source voltage plus the voltage across C. Since we assume that C and C1 are sufficiently large,

During switch-on period,

$Vc_0=V_1+Vc_1$ **(3)**

Therefore,

$Vc_0=V_1+[k/(1-k)]\ V_1=[1/(1-k)]\ V_1$

$V_0=Vc_0=[1/(1-k)]\ V_1$ **(4)**

The voltage transfer gain of continuous conduction mode (CCM) is:

$M=V_0/V_1=1/(1-k)$ **(5)**

The output voltage and current and the voltage transfer gain are:

$V_0=[1/(1-k)]\ V_1$

$I_0=(1-k)\ I1$

$M=1/(1-k)$

Average voltages and Average currents:

$Vc=kV_0$,

$Vc_1=V_0$.

$I_{L0}=I_0$,

$I_L=[1/(1-k)]\ I_0$.

RE-LIFT CIRCUIT

Re-lift circuit is derived from the self-lift circuit and it is shown in Figure 4. The circuit has additional voltage lift components i.e. extra capacitor and inductors in addition to that of the self-lift circuit.

Re-lift circuit performs a positive-to-positive DC-DC step up voltage conversion with high efficiency, high power density and cheap topology in a simple structure same as that of the self-lift circuit, but comparatively high voltage transfer ratio. The output voltage and current of this converter are smooth.

Two capacitors are applied to lift the output voltage by twice of the input voltage. The output voltage of the re-lift converter is double that of the self-lift converter. It consists of a static switch S, diodes D, D_1, D_2, D_{10} and D_{11}, three inductors L, L_1 and L_0, three capacitors C, C_1 and C_2, and the output capacitor C_0. Compare with the self-lift circuit it can be seen that there is additional one capacitor C_2, one Inductor L_3 and two diode D_1 and D_2 added into the re-lift circuit. Capacitor C2 performs the function to lift the capacitor voltage Vc by twice of source voltage V_S.

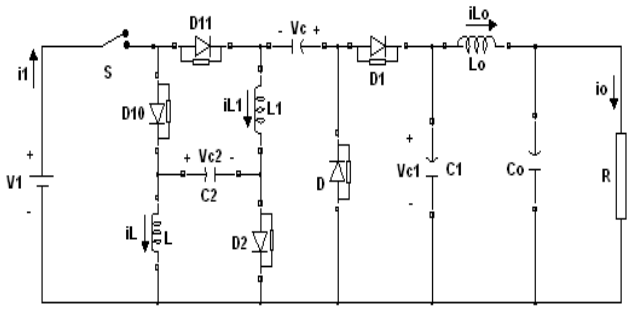

Figure 4: Re-Lift Topology.

Circuit Operation

When switch S is ON, its equivalent circuit is shown in Figure 5. The source instantaneous current is equal to $i_{L1}+i_{L2}+i_{C1}+i_{L3}+i_{C2}$. Inductor L_1 and L and capacitor C_2 absorbs energy from the source. Simultaneously inductor L_0 absorbs energy from source and capacitor C. Both currents i_{L1} and i_{L2} increase during switch-ON period. The addition of input voltage and the capacitor voltage Vc that is stored in it during switch-OFF period supply the load current.

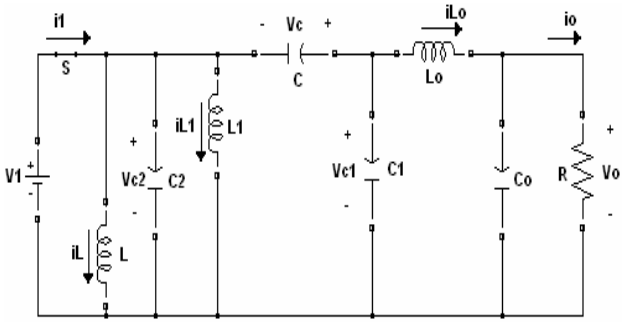

Figure 5: Switch-ON Equivalent Circuit.

When Switches S is turned OFF its equivalent circuit is shown in Figure 6. The source current is equal to zero. The stored energy in the inductors L_1 and L and the capacitor C_2 discharges and charge the capacitor C with the direction as shown in the figure 3.4. Simultaneously current i_{L0} flows through the load, which is sustained by the inductor L_0. Both currents i_{L1} and i_{L2} decreases during switch-OFF period.

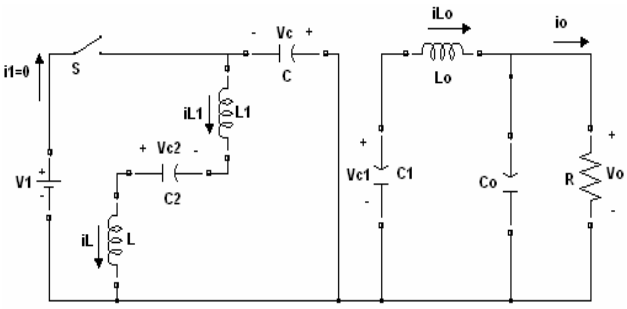

Figure 6: Switch-OFF Equivalent Circuit.

Analysis of Proposed Circuit Re-Lift

Under steady state, the average inductor voltages over a period are zero. Thus,

$$V_{C0}=V_0 \qquad \textbf{(6)}$$

Since we assume C_2 is large enough and the source voltage V_1 biases C_2 during switch on period, thus,

$$V_{C2}=V_1 \qquad \textbf{(7)}$$

During switch-on, the other capacitor voltage equation can also be derived since we assume all the capacitor to be large enough,

$$V_0=V_{C_1}=V_C+V_1 \qquad \textbf{(8)}$$

The inductor current I_L, increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_1 and $-V_{L\text{-}OFF.}$ Therefore,

$$KTV_1=(1-k)\,TV_{L\text{-}OFF}$$

Hence,

$$V_{L\text{-}OFF}=[k/(1-k)]\,V_1 \qquad \textbf{(9)}$$

The inductor current I_{L1} increase in the switch-on period and decreases in the switch-off period. The corresponding voltages across L_1 are V_1 and $-V_{L1\text{-}OFF.}$

$$KTV_1=(1-k)\,TV_{L1\text{-}OFF}$$

$$V_{L1\text{-}OFF}=[k/(1-k)]\,V_1 \qquad \textbf{(10)}$$

From switch-off period equivalent circuit,

$$V_C=V_{C\text{-}OFF}=V_{L\text{-}OFF}+V_{L1\text{-}OFF}+V_{C_2}$$

$$V_C=[(1+k)/(1-k)]\,V_1$$

$$V_0=V_C+V_1$$

$$V_0=[2/(1-k)]\,V_1. \qquad \textbf{(11)}$$

The voltage transfer gain of continuous conduction mode (CCM) is:

$$M_R=V_0/V_1=2/(1-k) \qquad \textbf{(12)}$$

Average voltages:

$$V_C=[(1+k)/(1-k)]\,V_1$$

$$V_{C_1}=V_0=V_{C_0}$$

$$V_{C_2}=V1s$$

Average currents:

$$I_{L0}=I_0,$$

$$I_L=[1/(1-k)]\,I_0.$$

CLOSED LOOP CONTROLLER FOR PROPOSED CONVERTER TOPOLOGIES

Closed Loop control scheme for the proposed self-lift DC-DC converter topology is shown in the above Figures 7 and 8. The control scheme essentially consisting of only one voltage sensor with simple control structure when compared with conventional DC-DC boost converter which requires both voltage and current sensors. DC voltage of the load is fed back and compared with V_{dc} reference voltage and the error is given to the PI controller to stabilize the error and the signal obtained from the controller is the modulating signal for the PWM scheme. Signal from the PI

controller is compared with high frequency ramp signal to produce required pulse for the N-channel MOSFET switch to obtain the reference DC voltage at the load.

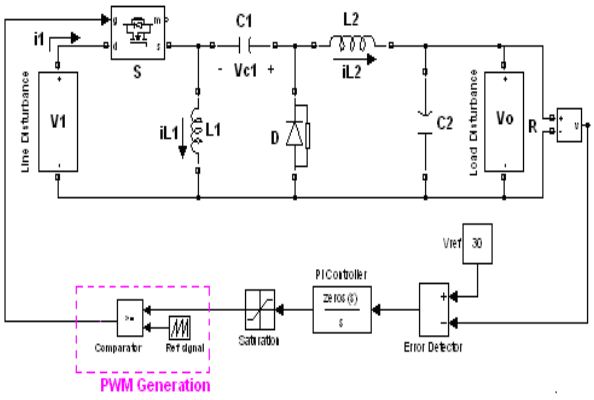

Figure 7: SELF-LIFT Circuit with PI-Controller.

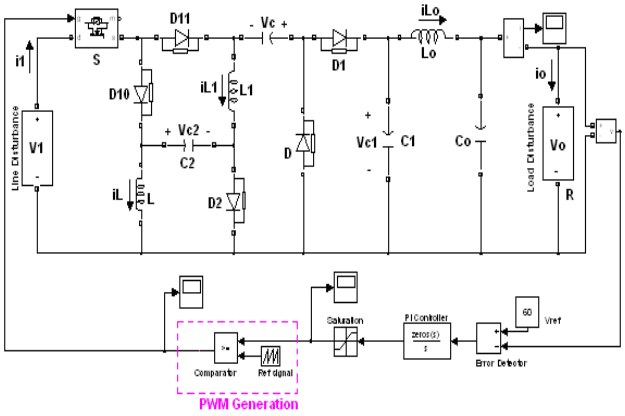

Figure 8: RE-LIFT Circuit with PI-Controller.

This work concentrates the absolute values rather than polarity in the following description and calculations. The directions of all voltages and currents are defined and shown in Figures 7 and 8. It is assumed that all the components are ideal and the capacitors are large enough. It is assumed that the circuits operate in continuous conduction mode. The output voltage and current are Vo and I_0 the input voltage and current are V_I and I_1.

SIMULATION RESULTS AND DISCUSSION

Simulation Parameters Taken for Analysis

Input Voltage V_1	= (10 - 9) volts
Inductance	= 100µH
Capacitance	= 5µF
Load Resistance	= (5 - 7) ohms.
Switching Frequency	= 50 KHz.

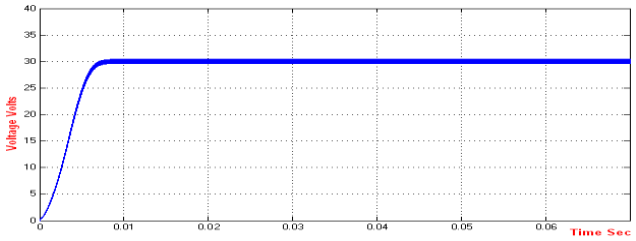

Figure 9: Fixed Output DC Voltage for Self-Lift.

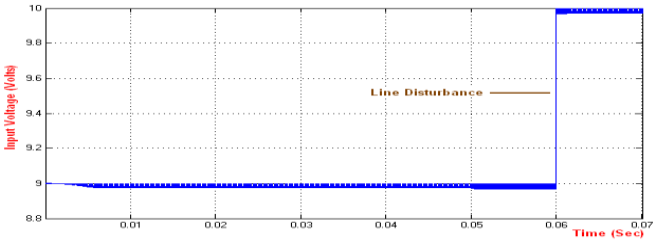

Figure 10: Input DC Voltage for Self-Lift.

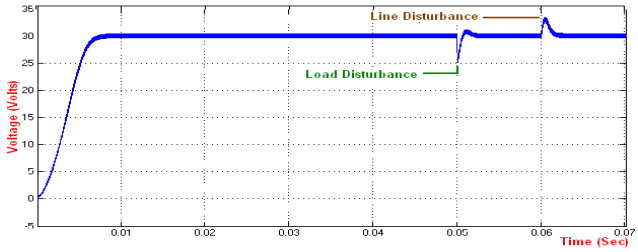

Figure 11: Fixed Output DC Voltage for Self-Lift.

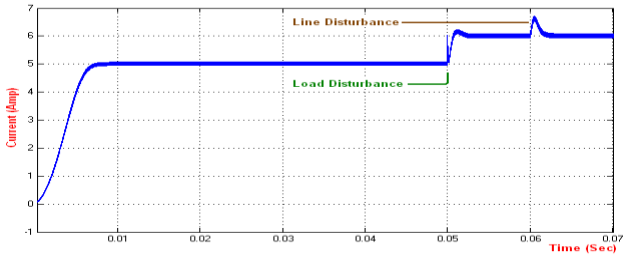

Figure 12: Output DC Current for Self-Lift.

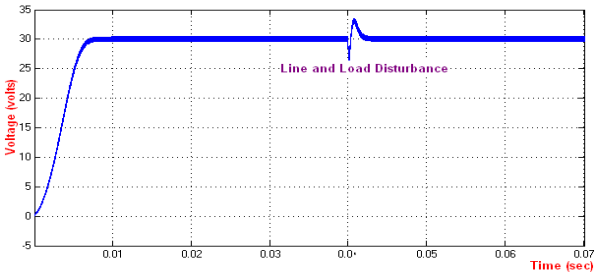

Figure 13: Fixed Output DC Voltage for Self-Lift.

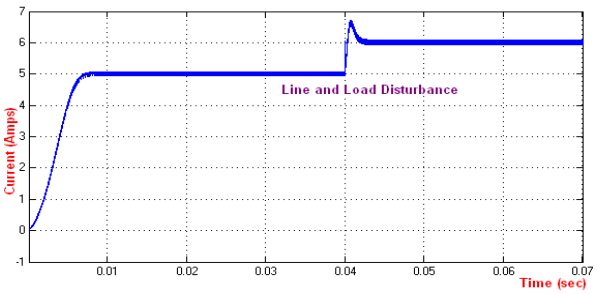

Figure 14: Fixed Output DC Current for Self-Lift.

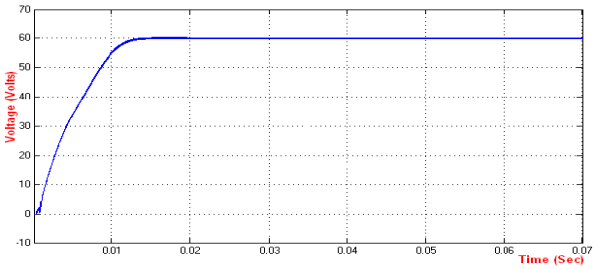

Figure 15: Fixed Output DC Voltage for Re-Lift.

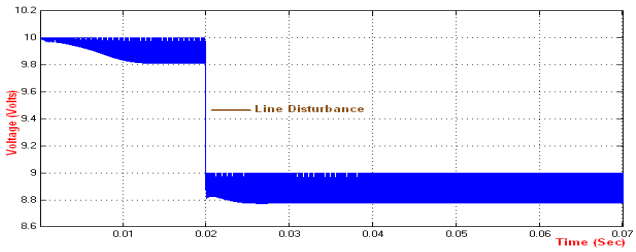

Figure 16: Input DC Voltage for Re-Lift.

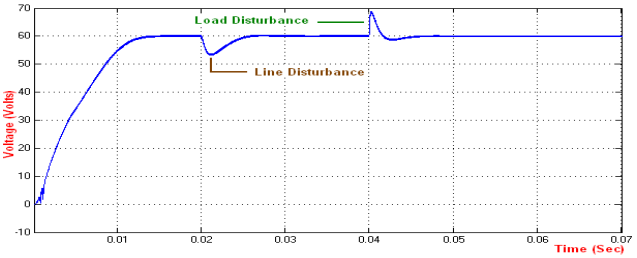

Figure 17: Fixed Output DC Voltage Re-Lift.

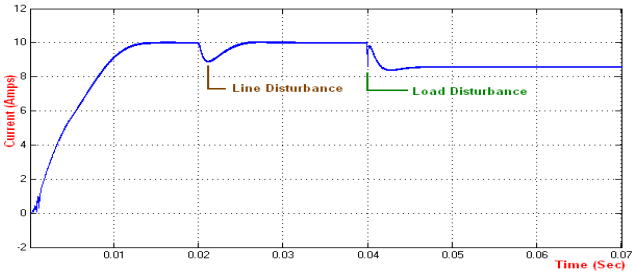

Figure 18: Output DC Current Re-Lift.

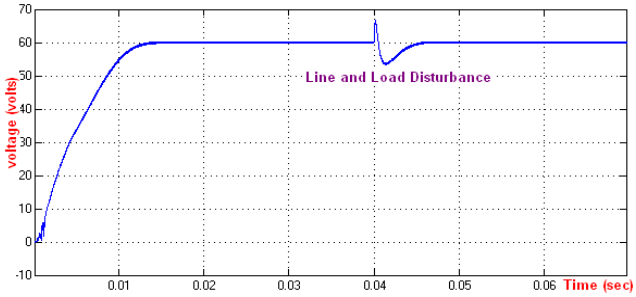

Figure 19: Fixed Output DC Voltage Re-Lift.

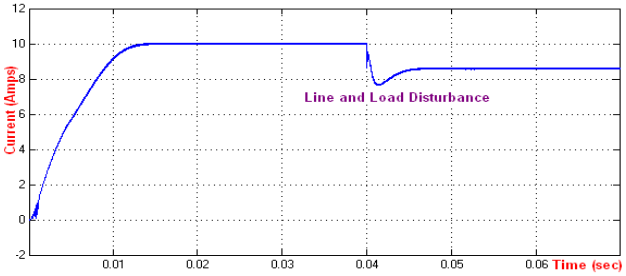

Figure 20: Output DC Current for Re-Lift.

Figure 9: Implies the output voltage for Self-lift topology and provides a fixed DC output voltage of 30 Volts. The settling time for this output voltage is less than 0.01 sec.

Figure 10: Shows the input DC voltage applied to Self-lift topology. Initially 9 Volts is maintained and introduced a change to 10 Volts at 0.06 Sec, for analyzing the line disturbance performance.

Figure 11: Depicts the output voltage for Self-lift topology and provides a fixed DC output voltage of 30 Volts under both line and load disturbance. Hence the circuit provides stabilized output under distortion conditions. Line disturbance applied at 0.06 Sec and load disturbance applied at 0.05 Sec.

Figure 12: Illustrates the load current for Self-lift topology under line and load disturbance. As load

resistance decreases from 6Ω to 5Ω the load current increases from 5A to 6A.

Figure 13: Depicts the output voltage for Self-lift topology and provides a fixed DC output voltage of 30 Volts under both line and load disturbance introduced at the same time. Hence the circuit provides stabilized output under distortion conditions. Both disturbances are introduced at 0.04 sec.

Figure 14: Indicates the load current for Self-lift topology under line and load disturbance introduced at the same time. As load resistance decreases from 6Ω to 5Ω the load current increases from 5A to 6A.

Figure 15: Implies the output voltage for Re-lift topology and provides a fixed DC output voltage of 60 Volts. The settling time for this output voltage is less than 0.01 sec.

Figure 16: Shows the input DC voltage applied to Re-lift topology. Initially 10 Volts is maintained and introduced a change to 9 Volts at 0.02 Sec, for analyzing the line disturbance performance.

Figure 17: Depicts the output voltage for Re-lift topology and provides a fixed DC output voltage of 60 Volts under both line and load disturbance. Hence the circuit provides stabilized output under distortion conditions. Line disturbance applied at 0.02 Sec and load disturbance applied at 0.04 Sec.

Figure 18: Illustrates the load current for Re-lift topology under line and load disturbance. As load resistance increases from 6Ω to 7Ω the load current decreases from 10A to 8.57A.

Figure 19: Depicts the output voltage for Re-lift topology and provides a fixed DC output voltage of 60 Volts under both line and load disturbance introduced at the same time. Hence the circuit provides stabilized output under distortion conditions. Both disturbances are introduced at 0.04 sec.

Figure 20: Indicates the load current for Re-lift topology under line and load disturbance introduced at the same time. As load resistance increases from 6Ω to 7Ω the load current decreases from 10A to 8.57A.

CONCLUSIONS

This paper analyzed a successful utilization of Voltage lift technique to a new series of Luo DC-DC Boost Converter Topologies with simplified control strategy. The simulation results are compared with the theoretical analysis and verified.

All Luo-Converters implementing the voltage-lift technique, avoid taking too high value of the conduction duty k, overcomes the effects of parasitic elements and increases the output voltage of the DC-DC converters. In the analyzed boost converters only one controlled is utilized whereas in conventional boost converters require two closed controllers. Hence the redundancy of the analyzed converter is reduced.

Finally, it can be concluded that Luo converters topologies are modern boost converter to replace conventional DC-DC boost converter. This converter found application in hardware, car auxiliary power supplies, industrial applications, servomotor drives, medical equipment, and a high efficiency, widely adjustable high voltage regulated power supply (HVRPS).

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